# Evaluating the ADM1 260 Super Sequencer with Interchip Bus and Nonvolatile Fault Recording 

## FEATURES

Full functional support evaluation kit for the ADM1260
$I^{2} C$ interface supports all device related software
Interchip bus simplifies multidevice cascading and sequencing operation
10 adjustable voltages reference for input emulation
Switch controlled, open-drain/push-pull digital inputs Extra headers for easy probing Includes point to point patch cables for easy wiring

EVAL-ADM1260EBZ EVALUATION KIT CONTENTS
EVAL-ADM1260CSZ evaluation board and sample silicons ADM1260 device socket

8-way, 100 mm micro match ribbon cable Patch cables

## ADDITIONAL HARDWARE NEEDED <br> USB to $I^{2} C$ dongle USB-SDP-CABLEZ <br> 9 V to 14.4 V power supply

SOFTWARE NEEDED
ADI Power Studio

## GENERAL DESCRIPTION

The EVAL-ADM1260CSZ is a compact, full-feature evaluation board for the ADM1260 that comes in the EVAL-ADM1260EBZ evaluation kit.

Ten programmable driver outputs, Pins PDO1 to PDO10 (PDOx), and five dual-function inputs, Pins VX1 to VX5 (VXx), along with five selectable input attenuators that allow supervision of supplies, Pins VP1 to VP4 (VPx), and Pin VH give users flexibility and allows a wide range of application setups.

Ten LEDs give users direct visual indication on variations in the input board status. There is one LED to indicate the board power supply status.
The switches on the board allow the user to change the device address easily.

The evaluation kit supports $\mathrm{I}^{2} \mathrm{C}$ communication, allowing users to communicate with the ADM1260 devices. The evaluation kit also supports cascade setup so multiple evaluation boards can connect and share the same $\mathrm{I}^{2} \mathrm{C}$ bus.

The EVAL-ADM1260CSZ is fully compatible with the ADI Power Studio ${ }^{\text {m" }}$ software, to download this software, go to the ADM1260 product page.

Users need a USB-SDP-CABLEZ dongle to use the evaluation software tools. Only one dongle is required in a multiboard cascade setup. One device socket is included in each kit. The ADM1260 data sheet provides additional information and must be consulted when using the evaluation board.

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## REVISION HISTORY

## 4/16-Revision 0: Initial Version

## EVALUATION BOARD PHOTOGRAPH AND COMPONENTS

See Figure 1 for the numbers described in Table 1.


Figure 1. Evaluation Board Components
Table 1. Components Required for Evaluating the ADM1260 (See Figure 1)

| Number | Component | Description |
| :---: | :---: | :---: |
| 1 | Multiple board connector | Connects up to four ADM1260 evaluation boards together. The connector carries SMBus lines, ICB lines, and power across all the boards connected. |
| 2 | Rotating potentiometer | Varies the output voltage of the regulators, which is connected to the voltage sensing pins of the ADM1260. |
| 3 | Voltage regulator enable selection | Selects the enable signal for the voltage regulators. There are three selection options: the bottom position selects the enable signal from the PDOx pins; the middle position turns off the voltage regulator manually; and the top position enables the voltage regulator manually. |
| 4 | Range selection for VPx pins | Selects the high or low range for the VPx pins. Position A and Position B on the board denotes Position H and Position, L, respectively. |
| 5 | Address selection switches | Selects the SMBus address for the ADM1260. For more details, refer to Table 3. |
| 6 | DAC outputs | These are the DAC outputs on the ADM1260. These pins can connect to the feedback node of the voltage regulators for margining. |
| 7 | ICB pull-up switch | Always set this to EN (bottom position) to pull up the ICB lines. |
| 8 | Chip power switch | This switch powers the chip using 12 V or connects to the VH voltage regulator. |
| 9 | Socket | ADM1260 silicon is placed in the socket and gives the user easy replaceability. |
| 10 | $1^{2} \mathrm{C}$ dongle connector | Connects the USB-SDP-CABLEZ dongle to the board for programming the ADM1260 ( ${ }^{2} \mathrm{C}$ dongle must be purchased separately). |
| 11 | Power adapter connector | Connect the power adapter connector to the wall power adapter to power the evaluation board. |
| 12 | Bench power supply connector | Connects the bench power supply to power up the board. |
| 13 | Switch for digital inputs | Emulates digital inputs. |

## EVALUATION BOARD DESCRIPTION

The EVAL-ADM1260CSZ evaluation board is designed for evaluating the ADM1260 Super Sequencer ${ }^{\ominus}$ IC. The board is easy to use, easy to probe, allows flexible wiring, and is capable of supporting large mutltidevice systems by cascading multiple boards.

## SUPPORTED DEVICES

The evaluation board is designed to support the ADM1260 when the silicon is placed in the SOCKET-ADM106XLFZ daughter card.

## POWER SUPPLIES

The evaluation board can accept 9 V to 14.4 V from a bench power supply through Connector J5-1 and Connector J5-2. It also supports a wall mountable switching power supply with the voltage range 9 V to 14.4 V using Connector J6. Connector J6 is grounded and has reverse voltage protection circuits to prevent damage due to incorrect polarity. The current consumption of a single board depends on the exact configuration of the board and sequence, but the consumption is typically less than 200 mA .

## INPUTS EMULATION

Ten on-board adjustable voltage regulators from Analog Devices provide input supply emulation for all different setups supported by the ADM1260.
Each regulator operates independently and the output voltages can be easily adjusted by hand using an on-board, rotating potentiometer.

Every regulator can be enabled or disabled by the user or by the ADM1260 device, depending on the selection switch configuration. There is an LED to indicate the on/off status for each regulator.
All regulators have a feedback pin that allows the user to evaluate the margining function of the ADM1260.

An additional on-board, two-way, push-pull/open-drain switch, S13, can emulate digital inputs, if required.

## OUTPUT SIGNAL

PDOx output signals from the ADM1260 can easily connect to the regulator enabled control circuits on the board to control the on-board voltage regulators. The user can easily link the PDOx output signal to a regulator enable input by using the 10 switches S12 comprises. Linking the PDOx output signal to a regulator enable input allows the board to perform simulations for realworld sequencing applications.
The digital-to-analog converter (DAC) output signals can be wired to the feedback node of the regulators on the board to achieve supply margining.

The wiring of the DAC output to the feedback node of the regulator is made easy with the point to point patch cables included in the evaluation kit. The user can easily connect the DAC outputs of the ADM1260 to a regulator feedback node.

## $I^{2} \mathrm{C}$ INTERFACE

The evaluation board supports an $I^{2} \mathrm{C}$ interface. The user can connect the $\mathrm{I}^{2} \mathrm{C}$ end of the dongle from the PC USB port to the board using the USB-SDP-CABLEZ. The dongle has internal pull-ups for the SDA and SCL bus.

## MULTIPLE BOARD SETUP

Connector SK2, Connector SK3, and the eight-way ribbon cable allow up to four EVAL-ADM1260CSZ boards to connect to evaluate complex cascade sequencing setups.

A connection cable carries power and the interchip bus (ICB) to every board that is connected together. The user must only connect the power and the USB-SDP-CABLEZ to one board. It is recommended to connect the power supply to the board in the middle of a multiple board setup to ensure even power dissipation in the traces/cables.


Figure 2. Multiple Boards Connection

## MARGINING GUIDE

The ADP7102 LDO in the evaluation board provides adjustable VXx and VPx input voltages to the VXx and VPx pins.

The DAC1, DAC2, and DAC3 outputs, labeled on the board as $\mathrm{X} 1, \mathrm{X} 2$, and X 3 , are designed for VXx supply margining to the board. The DAC4 and DAC5 outputs, labeled on the board as X4 and X5, are designed for VPx supply margining. DAC6, labeled on the board as X 6 , is designed for VH supply margining.

For margining the supplied voltage, the output of the DACs must connect to the feedback node of the LDOs. The connectors to the VXx feedback nodes are labeled T1 to T5, the VPx feedback nodes are labeled T7 to T10, and the VH feedback node is labeled T6.

The reference voltage of the ADP7102 is 1.22 V , so the midcode of the DACs must be set as 1.25 V to achieve the highest maximum and minimum range for margining the rails.


Figure 3. ADP7102 Functional Diagram

## QUICK START GUIDE

## HARDWARE SETUP

1. Put Jumpers J1, J2, J3, and J4 into Position H on the board. This puts the output of the VPx regulators to higher voltage ranges.
2. All the jumpers comprised in the J5 jumper must be populated since J 5 connects the output of the voltage regulator to the respective input pins, VPx, VXx, and VH, of the sequencer.
3. Put Switches S1 to S10 into the bottom position. This enables the voltage regulators connected to the Pin VXx and Pin VPx input to be controlled by an external signal such as the PDOx pins of the ADM1260.
4. Set all the switches S 12 comprises to the on position which connects the PDOx pins to the enable pins, EN-VXx, ENVPx, and EN-VH, of the LDO in the board of the voltage regulator as shown in Table 2.

Table 2 PDOx Mapping

| Connection Point | Connected To |
| :--- | :--- |
| PDO1 | EN-VX1 |
| PDO2 | EN-VX2 |
| PDO3 | EN-VX3 |
| PDO4 | EN-VX4 |
| PDO5 | EN-VX5 |
| PDO6 | EN-VP1 |
| PDO7 | EN-VP2 |
| PDO8 | EN-VP3 |
| PDO9 | EN-VP4 |
| PDO10 | EN-VH |

5. Set Switch S11 to EN, enabling pull-up on the ICB bus and set Switch S14 to PWR so the VH pin on the ADM1260 is directly connected to the supply voltage, 12 V .
6. Set the SMBus address to the required address. Table 3 shows the configuration for Switches A0 and A1 for different addresses.

Table 3. SMBus Address Configuration

| Address | A1 |  |  |  | A0 |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  | $\mathbf{1}$ | $\mathbf{2}$ | $\mathbf{3}$ | $\mathbf{4}$ | $\mathbf{1}$ | $\mathbf{2}$ | $\mathbf{3}$ | $\mathbf{4}$ |
|  | On | Off | Off | Off | On | Off | Off | Off |
| $0 \times 35$ | On | Off | Off | Off | Off | Off | Off | On |
| $0 \times 36$ | Off | Off | Off | On | On | Off | Off | Off |
| $0 \times 37$ | Off | Off | Off | On | Off | Off | Off | On |

## SOFTWARE GRAPHICAL USER INTERFACE (GUI)

## Overview

ADI Power Studio is a free software tool for programming and configuring the ADM1260. It can be downloaded from the ADM1260 product page on the Analog Devices website. The software package includes a GUI evaluation tool and a USB to the USB-SDP-CABLEZ I ${ }^{2} \mathrm{C}$ dongle driver.

## GUI Installation

Connect the USB cable to the dongle only after the software installs.

1. Install the ADM1260 software GUI. Double-click the ADI Power Studio vx.x.x.x Setup.exe installation file to start the installation.
2. When the License Agreement window appears, click I Agree to continue.
3. In the ADI Power Studio Setup: Installation Options window, see Figure 4, ADI Power Studio (required), USB-SDP-CABLEZ Driver, and Create Start Menu Shortcuts are preselected. If the USB-SDP-CABLEZ driver is already installed, uncheck the USB-SDP-CABLEZ Driver checkbox.

- ADI Power Studio Setup: Installation Options

| 0 | $\square$ | $X$ |
| :--- | :--- | :--- |

Check the components you want to install and uncheck the components you don't want to install. Click Next to continue.


Figure 4. Installation Options
4. In the ADI Power Studio Setup: Installation Folder window, there is an option to select a custom installation location, as seen in Figure 5. Click Browse to navigate to the preferred installation location (optional). Click Install to install the GUI onto the computer.


Space required: 34.9 MB
Space available: 103.6 GB


Figure 5. Installation Location
5. When the progress bar is $100 \%$ after clicking Install and says Completed, click Close to finish the installation process; see Figure 6.


Figure 6. Installation Complete Window

## Loading the Demo Configuration

Connect the evaluation board to the computer using the USB-SDP-CABLEZ I ${ }^{2} \mathrm{C}$ dongle. Launch the ADI Power Stuido software by clicking Start Menu > All Programs > Analog Devices > ADI Power Studio vX.Y.Z > ADI Power Studio.

In Figure 7, when the GUI launches, a pop-up window shows the $\mathrm{I}^{2} \mathrm{C}$ dongle and the ADM1260 is detected. Click OK to proceed. For a single board demo, ensure the device address is set to $0 \times 34$; for a two board demo, set the device address to $0 \times 34$ and $0 \times 35$.


Figure 7. Connecting the to the ADM1260

In the Welcome tab, Figure 8, click Open Project and navigate to the location where the demo files are located and select the *.ssp demo file. To download the demo configuration files, go to the ADM1260 product page.


Figure 8. Welcome Tab
If the configuration on the connected ADM1260 is different than the configuration file that is being loaded, a pop-up window appears; see Figure 9. Click Yes to program the device.


Figure 9. Device Program Pop-Up Window
Once the device or devices are progmrammed, the sequence atuomatically runs. To see the sequence configuration, click Sequencing on the top menu, which opens the Sequence and State Configuration window in Figure 10.


Figure 10. Sequence and State Configuration Window

The input undervoltage (UV) and overvoltage (OV) thresholds can be modified by clicking the Hardware Configure tab and selecting the Supply Rails tab. The Supply Rails tab, as seen in Figure 11, shows a summary of all the voltage inputs and the PDOx outputs used for enabeling the voltage rails. The supply monitor configuration, such as OV, UV, and PDOx, can be modified in the Properties menu on the right side of the window.


Figure 11. Supply Rails Tab

Real-time voltage reading and the status for the supplies can be read back in the Pin Status Monitor tab, Figure 12, which can be accessed under the Monitor menu.


Figure 12. Pin Status Monitor Tab

## DEMONSTRATION CONFIGURATION

To download the demo configuration files, go to the ADM1260 product page. The file contains two configuration files: one demonstrates the single device functionality of the ADM1260 and the other demonstrates multiple device functionality of ADM1260.

## DEMO 1: SINGLE BOARD SEQUENCING

In this demonstration, the PDOx signals are turned on one by one by the sequence configuration to enable the voltage regulators. The VXx rails are the first to come up followed by the VPx rails. The ADM1260 is powered by the VH rails in this particular demo, which is done by setting Switch S14 to PWR. Set the device address to $0 \times 34$; refer to Table 3 for more information.
The sequence engine turns on a rail and checks if that particular rail has either an undervoltage (UV) or overvoltage (OV) fault. If there is no fault in the rail for 200 ms , the sequence proceeds to the next rail until all the rails are up. If either the UV or OV fault persists in the rails that the sequence engine is trying to sequence, the sequence engine times out after 400 ms and tries to sequence all the rails again.
If a fault happens in any of the rails that are already powered up while the sequence engine is sequencing or is in the power good state, the sequence engine jumps to the power fail state and tries to sequence the rails. In the power fail state, the ADM1260 does a black box write.
The OV thresholds are set to 1.30 V for the VXx pins and 3.5 V for the VPx pins. UV thresholds are set to 1.00 V for the VXx pins and 3.1 V for the VPx pins. For the demonstration configuration to sequence as expected, the voltage for the VXx pins and VPx pins must be set in within the UV and OV thresholds.

## DEMO 2: MULTIPLE BOARD SEQUENCING (TWO BOARDS)

This demonstration shows sequencing across three boards and the function of ICB bus. Three boards must connect serially using the SK2 and SK3 ports. The boards must have an SMBus address of $0 \times 34$ and $0 \times 35$. When multiple evaluation boards are connected together, only one $\mathrm{I}^{2} \mathrm{C}$ dongle and power source is required since the serial connecting cable carries the power, the $\mathrm{I}^{2} \mathrm{C}$ lines, and the ICB lines across the boards.

The sequence configuration for this demo enables the PDOx signals one by one to enable the LDOs. The VXx rails on the ADM1260 are the first to come up followed by the VPx rails. The sequence configuration is made to enable one rail per device in every state, showing the robustness of multidevice sequencing. The sequence enables Pin VX1 on Device 0x34, followed by Pin VX1 on Device 0x35, Pin VX2 on Device 0x34, and so on.
The sequence engine turns on a rail and checks if that particular rail has a UV or OV fault. If there is no fault for 200 ms , the sequence engine proceeds to the next rail until all the rails are powered up on the three boards. If either the UV or OV fault persists in the rail that the sequence engine is trying to sequence, the sequence engine times out after 400 ms and tries to sequence all the rails again.
If a fault happens in any of the rails that are already powered up while the sequence engine is sequencing or in the power good state, all three devices jump to the power fail state and try to sequence the rails again.
The OV thresholds are set to 1.30 V for the VXx pins and 3.5 V for the VPx pins. The UV thresholds are set to 1.00 V for the VXx pins and 3.1 V for the VPx pins. For the demonstration configuration to sequence as expected, the voltage for the VXx pins and VPx pins must be set in between the UV and OV thresholds.

## SWITCH, JUMPER, AND LED FUNCTIONS

Table 4. Switch Functions

\begin{tabular}{|c|c|c|c|}
\hline Designator \& Switch \& Description \& Default \\
\hline A0 \& \[
\begin{aligned}
\& 1 \\
\& 2 \\
\& 3 \\
\& 4
\end{aligned}
\] \& \begin{tabular}{l}
Device address switch AO. \\
On: Address Pin A0 pulled down to ground. \\
On: Address Pin A0 pulled down to ground through a \(150 \mathrm{k} \Omega\) resistor. \\
On: Address Pin AO floating to allow maximum leakage current. \\
On: Address Pin A0 pulled up to VDDCAP through a \(150 \mathrm{k} \Omega\) resistor.
\end{tabular} \& \begin{tabular}{l}
On \\
Off \\
Off \\
Off
\end{tabular} \\
\hline A1 \& \[
\begin{aligned}
\& 1 \\
\& 2 \\
\& 3 \\
\& 4
\end{aligned}
\] \& \begin{tabular}{l}
Device address switch A1. \\
On: Address Pin A1 pulled down to ground. \\
On: Address Pin A1 pulled down to ground through a \(150 \mathrm{k} \Omega\) resistor. \\
On: Address Pin A1 floating to allow maximum leakage current. \\
On: Address Pin A1 pulled up to VDDCAP through a \(150 \mathrm{k} \Omega\) resistor.
\end{tabular} \& \begin{tabular}{l}
On \\
Off \\
Off \\
Off
\end{tabular} \\
\hline S13 \& 1

2 \& \begin{tabular}{l}
Optional digital input switch. <br>
Use in conjunction with X49. <br>
X49 connected: push-pull. <br>
X49 disconnected: open-drain. <br>
On: X49 pulled to ground. <br>
Off: X49 pulled to $3.3 \mathrm{~V} /$ high impedance. <br>
Use in conjunction with X32. <br>
X32 connected: push-pull. <br>
X32 disconnected: open-drain. <br>
On: X32 pulled to ground. <br>
Off: X32 pulled to 3.3 V/high impedance.

 \& 

Disconnected Disconnected Off Off <br>
Disconnected Disconnected Off Off
\end{tabular} <br>

\hline S11 \& Not applicable \& | Controls the cascade bus pull-up. |
| :--- |
| Position EN: pull-up ICB data CDA and clock CCL line to 3.3 V . |
| Position DIS: keep cascade bus data and clock line floating. | \& Postion EN <br>


\hline S1 to S10 \& Not applicable \& | Regulator control switch. |
| :--- |
| Position Top: regulator always on. |
| Position Middle: regulator shutdown. |
| Position Bottom: regulator controlled by the PDOx output signal of the ADM1260. | \& Position bottom <br>

\hline S14 \& Not applicable \& Controls the source voltage connected to the VH pin of the ADM1260. Position VH: connect the VH pin to the on-board VH regulator. Position PWR: connect the VH pin directly to the board supply. \& Position PWR <br>
\hline S12 \& 1 to 10 \& Turn on the enable PDOx outputs of the ADM1260 to control the enabling/disabling of the regulators. \& On <br>
\hline
\end{tabular}

Table 5. Jumper Functions

| Jumper | Corresponding Regulator/Rails | Description | Default |
| :--- | :--- | :--- | :--- |
| J1 to J41 | VP1 to VP4 | Regulator output voltage divider control jumpers. <br> Position H: regulator output range 1.5 V to 6 V. <br> Position L: regulator output range 0.5 V to 1.5 V. <br> Unplugged: disconnect regulator output. | Position H |
| J 5 | $\mathrm{VXx} / \mathrm{VPx} / \mathrm{VH}$ | Connects the LDO outputs to the device inputs. | All 10 populated |
| $\mathrm{J40}$ | VXx/VPx/VH | Connector used for device inputs probing. | Not applicable |
| $\mathrm{J41}$ | PDOx | Connector used for device outputs probing. | Not applicable |

[^0]Table 6. Power Indication LED Functions ${ }^{1}$

| LED | Rails |
| :--- | :--- |
| D10 | VH |
| D1 | VX1 |
| D2 | VX2 |
| D3 | VX3 |
| D4 | VX4 |
| D5 | VX5 |
| D6 | VP1 |
| D7 | VP2 |
| D8 | VP3 |
| D9 | VP4 |
| D11 | Board 3V3 supply |

${ }^{1}$ On position indicates voltage on corresponding rail.
Table 7. Patching Through-Hole Connection Points

| Connection Points | Connected To | Description |
| :---: | :---: | :---: |
| VX1 | VX1 pin | Input Connection VX1. |
| VX2 | VX2 pin | Input Connection VX2. |
| VX3 | VX3 pin | Input Connection VX3. |
| VX4 | VX4 pin | Input Connection VX4. |
| VX5 | VX5 pin | Input Connection VX5. |
| VP1 | VP1 pin | Input Connection VP1. |
| VP2 | VP2 pin | Input Connection VP2. |
| VP3 | VP3 pin | Input Connection VP3. |
| VP4 | VP4 pin | Input Connection VP4. |
| VH | VH pin | Input Connection VH. |
| PDO1 | PDO1 pin | Output Connection PDO1. |
| PDO2 | PDO2 pin | Output Connection PDO2. |
| PDO3 | PDO3 pin | Output Connection PDO3. |
| PDO4 | PDO4 pin | Output Connection PDO4. |
| PDO5 | PDO5 pin | Output Connection PDO5. |
| PDO6 | PDO6 pin | Output Connection PDO6. |
| PDO7 | PDO7 pin | Output Connection PDO7. |
| PDO8 | PDO8 pin | Output Connection PDO8. |
| PDO9 | PDO9 pin | Output Connection PDO9. |
| PDO10 | PDO10 pin | Output Connection PDO10. |
| EN-VX1 | VX1 regulator | Connect the EN-VX1 enable circuit to the PDOx outputs directly to allow the devices to take control of the VX1 regulator. |
| EN-VX2 | VX2 regulator | Connect the EN-VX2 enable circuit to the PDOx outputs directly to allow the devices to take control of the VX2 regulator. |
| EN-VX3 | VX3 regulator | Connect the EN-VX3 enable circuit to the PDOx outputs directly to allow the devices to take control of the VX3 regulator. |
| EN-VX4 | VX4 regulator | Connect the EN-VX4 enable circuit to the PDOx outputs directly to allow the devices to take control of the VX4 regulator. |
| EN-VX5 | VX5 regulator | Connect the EN-VX5 enable circuit to the PDOx outputs directly to allow the devices to take control of the VX5 regulator. |
| EN-VP1 | VP1 regulator | Connect the EN- VP1 enable circuit to the PDOx outputs directly to allow the devices to take control of the VP1 regulator. |
| EN-VP2 | VP2 regulator | Connect the EN- VP2 enable circuit to the PDOx outputs directly to allow the devices to take control of the VP2 regulator. |
| EN-VP3 | VP3 regulator | Connect the EN- VP3 enable circuit to the PDOx outputs directly to allow the devices to take control of the VP3 regulator. |
| EN-VP4 | VP4 regulator | Connect the EN- VP4 enable circuit to the PDOx outputs directly to allow the devices to take control of the VP4 regulator. |


| Connection Points | Connected To | Description |
| :--- | :--- | :--- |
| EN-VH | VH regulator | Connect the EN-VH enable circuit to the PDOx outputs directly to allow the <br> devices to take control of the VH regulator. |
| X1 | DAC1 pin | DAC Output 1. <br> X2 <br> D3C Output 2. <br> X4 |
| DAC2 pin |  |  |
| X5 | DAC3 pin Output 3. |  |
| X6 | DAC4 pin | DAC5 pin |
| T6 | DAC6 pin Output 4. |  |
| DAC Output 5. |  |  |
| DAC Output 6. |  |  |

## SOCKET SELECTION GUIDE

Table 8.

| Model | Description | Corresponding Devices |
| :--- | :--- | :--- |
| SOCKET-ADM106XLFZ | ADM1260 daughter card | ADM1260 in LFCSP |

## EVALUATION BOARD SCHEMATICS AND ARTWORK




Figure 14. ADM1260 Evaluation Board Schematic, Page 2


Figure 15. ADM1260 Evaluation Board Schematic, Page 3


Figure 16. ADM1260 Evaluation Board Schematic, Page 4


Figure 17. ADM1260 Evaluation Board Schematic, Page 5

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 9.

| Reference Designator | Description | Manufacturer | Part Number | Stock Code |
| :---: | :---: | :---: | :---: | :---: |
| A0, A1 | Switch, dip, raised actuators, four-way | Omron Electornic Components | A6S-4104-H | FEC 1960899 |
| C1 | Aluminium electrolytic capacitor, Cease $C$, $10 \mu \mathrm{~F}, 35 \mathrm{~V}$ | Panasonic |  | FEC 9697012 |
| C2, C4, C14, C16, C18, C19, C23 to C26, C28 to C36, C40 to C42, C44 to C49 | Capacitors, MLCC, X7R, 1 ¢F, 16V, 0603 | AVX | 0603YC105KAT2A | FEC 1658870 |
| C3, C13, C17, C21, C22 | Capacitors, MLCC, X5R, $1 \mu \mathrm{~F}, 25 \mathrm{~V}, 0603$ | AVX | 06033D105KAT2A | FEC 1658868 |
| C5 to C8, C10, C43 | SMD capacitors, 220 pF | Phycomp | 223886715221 | FEC 430948 |
| C9, C11, C15 | 16 V , SMD tantalum capacitors, $10 \mu \mathrm{~F}$ | AVX | TAJB106K016R | FEC 498737 |
| C20, C27 | Capacitors, MLCC, X7R, 100 nF, 25 V, 0603 | AVX | 06033C104JAT2A | FEC 1740614RL |
| D1 to D11 | Green, 0805, chip LEDs | Kingbright | KP-2012SGC | FEC 1318243 |
| J1 to J4 | 3 -pin, 0.1 " pitch headers and shorting shunt inserted in Position H | Harwin | M20-9990346 and M7566-05 | FEC 1022249 and 150-411 |
| J5 | 20-pin ( $2 \times 10$ ) 0.1" pitch header |  | M20-9971046 | FEC 102-2229 |
| Q1, Q3 to Q11 | General purpose NPD, SMD transistors | NXP | BC850C | FEC 1081241 |
| Q2, Q12, Q13 | N -channel, enhancement mode, MOSFETs | Fairchild | NDS7002A | FEC 984-5437 |
| R1 to R10 | $3 / 8$ " square ( 10 mm ), single-turn potentiometer, $1 \mathrm{M} \Omega$ resistors | Vishay | 63M-T607-105 | FEC 9608290 |
| R11, R40, R61, R70 | Resistors, $62 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W0603162K | FEC 9331417 |
| R12 to R14, R16 | Resistors, $0805,49.9 \mathrm{k} \Omega, 1 \%$ | Vishay Dale | CRCW080549K9FKEA | FEC 1469934 |
| $\begin{aligned} & \text { R15, R34, R41, R62, R71, R80, } \\ & \text { R99, R110, R120 } \end{aligned}$ | Resistors, $270 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W06031270K | FEC 9330941 |
| R17, R19, R36, R43, R52, R63, R72, R81, R100, R111, R121 | Resistors, $10 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W0603110K | FEC 9330399 |
| R18, R20 | Resistors, $12 \mathrm{k} \Omega, 0.1 \mathrm{~W}, 1 \%, 0805$ | Multicomp | MC01W0805112K | FEC 9332502 |
| R21, R22, R58, R67, R76, R85, R104, R115, R125 | Resistors, $82 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W0603182K | FEC 9331573 |
| R23 | Resistor, RC11, 0805, $0 \Omega$ | Phycomp | 232273091002 | FEC 9233750RL |
| R24, R25 | Resistors, $680 \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W06031680R | FEC 9331441 |
| R26, R27 | Resistors, 0603, $100 \mathrm{k} \Omega$ | Vishay Draloric | CRCW0603100KFKEA | FEC 1469649 |
| R28, R39, R47, R54, R57, R66, R75, R84, R103, R114, R124 | Resistors, $390 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W06031390K | FEC 9331166 |
| R23 | Resistors, $3 \mathrm{k} \Omega$, $0.1 \mathrm{~W}, 1 \%$, 0805 | Multicomp | MC01W080513K | FEC 9332995 |
| R31, R60, R63, R78, R87 to R89, R97, R106, R107, R117, R118, R127, R128, R142, R146 | Resistors, 0603, 1\%, $0 \Omega$ | Multicomp | MC0063W06030R | FEC 9331662 |
| R33, R48, R49, R79, R98, R108, R119 | Resistors, $100 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W06031100K | FEC 9330402 |
| $\begin{aligned} & \text { R37, R44, R55, R64, R73, R82, } \\ & \text { R101, R112 } \end{aligned}$ | Resistors, $20 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W0603120K | FEC 9330771 |
| R38, R53, R74 | Resistors, 1 k $\Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W060311K | FEC 9330380 |
| J5-1 | Red, 4 mm , banana socket | Deltron | 571-0500 | FEC 150-039 |
| J5-2 | Black, 4 mm , banana socket | Deltron | 571-0100 | FEC 150-040 |
| J6 | 2.1 mm, dc barrell power connector | Farnell |  | FEC 224-959 |
| J11 | Header, shrouded, 10-way | Molex | 70246-1004 | FEC 1392408 |
| J40, J41 | Headers, one row, 10-way | Tyco Electronics | 1-826629-0 | FEC 3418376 |
| R46, R56 | Resistors, $1 \mathrm{M} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W060311M | FEC 9330410 |
| R65 | Resistor, $1.74 \mathrm{k} \Omega, 0.063 \mathrm{~W}, 1 \%, 0603$ | Multicomp | MC0063W060311K74 | FEC 1170810 |
| R83, R143 to R145 | Resistors, $150 \mathrm{k} \Omega, 0.1 \mathrm{~W}, 1 \%, 0805$ | Multicomp | MC01W08051150K | FEC 9332626 |


| Reference Designator | Description | Manufacturer | Part Number | Stock Code |
| :--- | :--- | :--- | :--- | :--- |
| R30, R32, R34, R36, R130, | Resistors, RC22H, 0603, 1 k $\Omega$ | Phycomp | 232270461002 | FEC 9238484 |
| R132, R134, R136, R138, R140 |  | Vishay Dale | CRCW06033K01FKEA | FEC 1469791 |
| R31, R33, R35, R129, R131, <br> R133, R135, R137, R139, R141 | Resistors, 0603, 3k01,1\% |  |  |  |
| S1 to S10 | SP3T slide switches | ALPS | STSSS9131 | FEC 1123876 |
| T1 to T10 | Headers, one-way, one row | FCI | $68000-101 \mathrm{HLF}$ | FEC 1835272 |

$1^{2} \mathrm{C}$ refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


## ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you


















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[^0]:    ${ }^{1} \mathrm{~J} 1$ corresponds to VP1, J2 corresponds to VP2, J3 corresponds to VP3, and J4 corresponds to VP4.

